Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An image processing system adapted to process image frames and comprising:

an image processing engine operative to perform object-independent processing corresponding to a first layer of the image processing system , said object independent processing being performed on a per-frame basis on source data from integral registers of said image processing engine and captured on a per-frame basis in said integral registers of said image processing engine without access to external memory for storage of image data in order to avoid memory bandwidth limits to generate a first set of processed data, said image processing engine further ~~adapted to include~~ comprising a plurality of parallel processors, each said parallel processor associated with only a single different one of pixels of an image frame; and

a post processing engine operative to directly receive the first set of processed data and to perform object-dependent processing corresponding to a second processing layer of the image processing system on the received first set of processed data thereby to generate a second set of processed data, said post processing engine further ~~operative to include~~ comprising an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1.

2. (Original) The image processing system of claim 1 wherein the plurality of processors of the image processing engine form a massively parallel processing system.

3. (Original) The image processing system of claim 2 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

4. (Original) The image processing system of claim 3 wherein the systolic array type massively parallel processing system is configured as a single-instruction multiple-data system.

5. (Original) The image processing system of claim 1 wherein each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

6. (Original) The image processing system of claim 1 further comprising:

an image capturing block.

7. (Original) The image processing system of claim 6 wherein the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed.

8. (Original) The image processing system of claim 7 further comprising:

a realignment buffer adapted to realign the data received from first and second analog-to-digital converters disposed in the image capturing block.

9. (Currently amended) A method for processing images:

performing object-independent processing corresponding to a first image processing layer, said first image processing layer being limited to one pixel per processor, pixel-related object independent data, said object independent processing being performed on a per-frame basis on source data from integral registers of an image processing engine and captured on a per-frame basis in said integral registers of said image processing engine without access to external memory for storage of image data in order to avoid memory bandwidth limits to generate a first set of processed data;

supplying the first set of processed data from said integral registers directly to a second processing layer;

performing object-dependent processing corresponding to the second processing layer on the received first set of processed data thereby to generate a second set of processed data; and

using an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1.

10. (Original) The method of claim 9 further comprising:

performing object independent processing by a plurality of processors that form a massively parallel processing system.

11. (Original) The method of claim 10 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

12. (Original) The method of claim 11 further comprising:

configuring the systolic array massively parallel processing system as a single-instruction multiple-data system.

13. (Original) The method of claim 12 wherein each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

14. (Original) The method of claim 13 further comprising:

capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed.

15. (Original) The method of claim 14 further comprising

converting analog data corresponding to the image frame to digital data; and

realigning the converted digital data.

16. (Previously presented) The method of claim 9 further comprising:

performing object composition, recognition and association corresponding to a third processing layer.

17. (Previously presented) The image processing system of claim 1 further comprising:

a processing engine adapted to perform object composition, recognition and association corresponding to a third processing layer of the image processing system.